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Inventor Name Search Result

Your Search was:

Last Name = THOME
First Name = BRYAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10301894	6948155	150	11/22/2002	LITTLE OFFSET IN MULTICYCLE EVENT MAINTAINING CYCLE ACCURATE TRACING OF STOP EVENTS	THOME, BRYAN
10301935	Not Issued	71	11/22/2002	Data trace compression map	THOME, BRYAN
10302025	7047451	150	11/22/2002	TRACING PROGRAM COUNTER ADDRESSES USING NATIVE PROGRAM COUNTER FORMAT AND INSTRUCTION COUNT FORMAT	THOME, BRYAN
10729190	Not Issued	161	12/05/2003	Apparatus and method for trace stream identification of a pause point in code execution sequence	THOME, BRYAN
10729191	Not Issued	41	12/05/2003	Apparatus and method for op code extension in packet groups transmitted in trace streams	THOME, BRYAN
10729196	Not Issued	71	12/05/2003	Apparatus and method for compression of the timing trace stream	THOME, BRYAN
10729214	Not Issued	95	12/05/2003	APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR DEBUG HALT SIGNAL	THOME, BRYAN
10729272	Not Issued	164	12/05/2003	APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF MULTIPLE TARGET PROCESSOR EVENTS	THOME, BRYAN
10729326	7225365	150	12/05/2003	APPARATUS AND METHOD FOR IDENTIFICATION OF A NEW SECONDARY CODE	THOME, BRYAN

				START POINT FOLLOWING A RETURN FROM A SECONDARY CODE EXECUTION	
10729327	7210072	150	12/05/2003	APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER PRIMARY CODE FLUSH FOLLOWING INITIATION OF AN INTERRUPT SERVICE ROUTINE	THOME, BRYAN
10729401	Not Issued	161	12/05/2003	Apparatus and method for identification of a primary code start sync point following a return to primary code execution	THOME, BRYAN
10729639	7237151	150	12/05/2003	APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR RESET	THOME, BRYAN
10729647	Not Issued	164	12/05/2003	APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER SECONDARY CODE FLUSH FOLLOWING A RETURN TO PRIMARY CODE EXECUTION	THOME, BRYAN
11383337	Not Issued	94	05/15/2006	TRACING PROGRAM COUNTER ADDRESSES USING NATIVE PROGRAM COUNTER FORMAT AND INSTRUCTION COUNT FORMAT	THOME, BRYAN
11383540	Not Issued	25	05/16/2006	Reissue an ID to a Data Log Even if the Same ID May Be Repeated	THOME, BRYAN
60434020	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of a pipeline flattener secondary code flush following a return to primary code execution	THOME, BRYAN
60434087	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of a pause point in a code execution sequence	THOME, BRYAN
60434105	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of a processor reset	THOME, BRYAN
60434119	Not	159	12/17/2002	Apparatus and method	THOME, BRYAN

	Issued			identification of a primary code start sync point following a return to primary code execution	
60434120	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of a pipeline flattener primary code flush following initiation of an interrupt service routine	THOME, BRYAN
60434122	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of a processor debug halt signal	THOME, BRYAN
60434125	Not Issued	159	12/17/2002	Apparatus and method for op code extension in packet groups transmitted in trace streams	THOME, BRYAN
60434172	Not Issued	159	12/17/2002	Apparatus and method identification of a new secondary code start point following a return from a secondary code execution	THOME, BRYAN
60434174	Not Issued	159	12/17/2002	Apparatus and method for trace stream identification of multiple target processor events	THOME, BRYAN
60434176	Not Issued	159	12/17/2002	Apparatus and method for compression of the timing trace stream	THOME, BRYAN
60681386	Not Issued	159	05/16/2005	Efficient protocol for encoding memory events using a generic encoding scheme	THOME, BRYAN
09981972	6512954	150	10/16/2001	IMPLANTABLE DEVICE AND PROGRAMMER SYSTEM WHICH PERMITS MULTIPLE PROGRAMMERS	THOME, BRYAN J.
10350749	6792311	150	01/24/2003	IMPLANTABLE DEVICE AND PROGRAMMER SYSTEM WHICH PERMITS MULTIPLE PROGRAMMERS	THOME, BRYAN J.
10919553	Not Issued	71	08/17/2004	Implantable device and programmer system which permits multiple programmers	THOME, BRYAN J.
11381688	Not Issued	25	05/04/2006	Systems And Methods For Multiplexing And Demultiplexing Multiple Data Sources	THOME, BRYAN J.
11640043	Not Issued	25	12/15/2006	Apparatus and method for encoding the execution of hardware loops in digital signal processors to optimize offchip export of diagnostic data	THOME, BRYAN J.

60677469	Not Issued	159	05/04/2005	Efficient merging data generated by multiple sources into a single data stream	THOME, BRYAN J.
60798510	Not Issued	159	05/08/2006	Method for encoding the execution of hardware loops in digital signal processor (DSP) such the export of this information offchip is optimized	THOME, BRYAN J.
09025123	5873894	150	02/17/1998	DIAGNOSTIC TEST PROTOCOL IN AN IMPLANTABLE MEDICAL DEVICE	THOME, BRYAN J.
09191808	6308099	150	11/13/1998	IMPLANTABLE DEVICE AND PROGRAMMER SYSTEM WHICH PERMITS MULTIPLE PROGRAMERS	THOME, BRYAN J.
11413406	Not Issued	30	04/27/2006	Method and system of a processor-agnostic encoded debug-architecture in a pipelined environment	THOME, BRYAN JOSEPH

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Inventor Name Search Result

Your Search was:

Last Name = SWOBODA
First Name = GARY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07718687	Not Issued	163	06/21/1991	PROCESSING SYSTEM, SYSTEM EMULATOR, MASK SETS, AND METHODS	SWOBODA, GARY
08443081	Not Issued	169	05/17/1995	SCAN DESIGN WITH CLOCKING SCHEME TO PERMIT BYPASS OPERATION	SWOBODA, GARY
09738241	6775793	150	12/15/2000	DATA EXCHANGE SYSTEM AND METHOD FOR PROCESSORS	SWOBODA, GARY
09887504	6931636	150	06/22/2001	MULTIPROCESSOR EMULATION SUPPORT USING DYNAMIC LINKING	SWOBODA, GARY
11855602	Not Issued	17	09/14/2007	Entry/Exit Control To/From a Low Power State in a Complex Multi Level Memory System	SWOBODA, GARY
60171392	Not Issued	159	12/21/1999	DATA EXCHANGE SYSTEM AND METHOD FOR PROCESSORS	SWOBODA, GARY
60186339	Not Issued	159	03/02/2000	Wire list walking	SWOBODA, GARY
60223697	Not Issued	159	08/08/2000	Multiprocessor emulation support using dynamic linking	SWOBODA, GARY
60795003	Not Issued	159	04/26/2006	Clock voting	SWOBODA, GARY
09481852	6567933	150	01/14/2000	EMULATION SUSPENSION MODE WITH STOP MODE EXTENSION	SWOBODA, GARY L
11383297	Not Issued	25	05/15/2006	System With Trace Capability Accessed Through the Chip Being Traced	SWOBODA, GARY L
11383300	Not Issued	30	05/15/2006	Using a Delay Line to Cancel Clock Insertion Delays	SWOBODA, GARY L

60747452	Not Issued	159	05/17/2006	BDX and CDX Formats	SWOBODA, GARY L
09273031	Not Issued	161	03/19/1999	PROCESSOR HAVING REAL-TIME EXTERNAL INSTRUCTION INSERTION FOR DEBUG FUNCTIONS WITHOUT A DEBUG MONITOR	SWOBODA, GARY L
60078786	Not Issued	159	03/20/1998	PROCESSOR HAVING REAL-TIME EXTERNAL INSTRUCTION INSERTION FOR DEBUG FUNCTIONS WITHOUT A DEBUG MONITOR	SWOBODA, GARY L
09481853	Not Issued	161	01/14/2000	Emulation system with peripherals recording emulation frame when stop generated	SWOBODA, GARY L.
09483237	6671665	150	01/14/2000	EMULATION SYSTEM WITH SEARCH AND IDENTIFICATION OF OPTIONAL EMULATION PERIPHERALS	SWOBODA, GARY L.
09483321	6836757	150	01/14/2000	EMULATION SYSTEM EMPLOYING SERIAL TEST PORT AND ALTERNATIVE DATA TRANSFER PROTOCOL	SWOBODA, GARY L.
09483367	6553513	150	01/14/2000	EMULATION SUSPEND MODE WITH DIFFERING RESPONSE TO DIFFERING CLASSES OF INTERRUPTS	SWOBODA, GARY L.
09483568	6564339	150	01/14/2000	EMULATION SUSPENSION MODE HANDLING MULTIPLE STOPS AND STARTS	SWOBODA, GARY L.
09483570	6820051	150	01/14/2000	SOFTWARE EMULATION MONITOR EMPLOYED WITH HARDWARE SUSPEND MODE	SWOBODA, GARY L.
09483697	6557116	150	01/14/2000	EMULATION SUSPENSION MODE WITH FRAME CONTROLLED RESOURCE ACCESS	SWOBODA, GARY L.
09740868	6754599	150	12/21/2000	DEBUG OUTPUT LOOSELY COUPLED WITH PROCESSOR BLOCK	SWOBODA, GARY L.
09740917	6868376	150	12/19/2000	DEBUG BI-PHASE EXPORT	SWOBODA, GARY

				AND DATA RECOVERY	L.
09740921	6725391	150	12/19/2000	CLOCK MODES FOR A DEBUG PORT WITH ON THE FLY CLOCK SWITCHING	SWOBODA, GARY L.
09741645	6388533	150	12/19/2000	Programmable ring oscillator	SWOBODA, GARY L.
09741647	6545549	150	12/19/2000	REMOTELY CONTROLLABLE PHASE LOCKED LOOP CLOCK CIRCUIT	SWOBODA, GARY L.
09798001	6708290	150	03/02/2001	CONFIGURABLE DEBUG SYSTEM WITH WIRE LIST WALKING	SWOBODA, GARY L.
09798173	6785850	150	03/02/2001	SYSTEM AND METHOD FOR AUTOMATICALLY CONFIGURING A DEBUG SYSTEM	SWOBODA, GARY L.
09798365	6928403	150	03/02/2001	AUTOMATIC DETECTION OF CONNECTIVITY BETWEEN AN EMULATOR AND A TARGET DEVICE	SWOBODA, GARY L.
09798425	6836882	150	03/02/2001	PIPELINE FLATTENER FOR SIMPLIFYING EVENT DETECTION DURING DATA PROCESSOR DEBUG OPERATIONS	SWOBODA, GARY L.
09798429	6754852	150	03/02/2001	DEBUG TRIGGER BUILDER	SWOBODA, GARY L.
09798555	7113902	150	03/02/2001	DATA PROCESSING CONDITION DETECTOR WITH TABLE LOOKUP	SWOBODA, GARY L.
09798595	6947884	150	03/02/2001	SCAN INTERFACE WITH TDM FEATURE FOR PERMITTING SIGNAL OVERLAY	SWOBODA, GARY L.
09798596	6859897	150	03/02/2001	RANGE BASED DETECTION OF MEMORY ACCESS	SWOBODA, GARY L.
09798606	6738929	150	03/02/2001	DYNAMICALLY CONFIGURABLE DEBUG PORT FOR CONCURRENT SUPPORT OF DEBUG FUNCTIONS FROM MULTIPLE DATA PROCESSING CORES	SWOBODA, GARY L.
09920180	7089437	150	08/01/2001	APPARATUS FOR DETERMINING POWER CONSUMED BY A BUS OF A DIGITAL SIGNAL	SWOBODA, GARY L.

				PROCESSOR USING CONUNTED NUMBER OF LOGIC STATE TRANSITIONS ON BUS	
09920193	Not Issued	161	08/01/2001	Apparatus and method for central processing unit power measurement in a digital signal processor	SWOBODA, GARY L.
09924800	6820222	150	08/08/2001	APPARATUS AND METHOD FOR PROCESSOR POWER MEASUREMENT IN A DIGITAL SIGNAL PROCESSOR USING TRACE DATA AND SIMULATION TECHNIQUES	SWOBODA, GARY L.
09924912	6795879	150	08/08/2001	APPARATUS AND METHOD FOR WAIT STATE ANALYSIS IN A DIGITAL SIGNAL PROCESSING SYSTEM	SWOBODA, GARY L.
09938201	6539497	150	08/22/2001	IC WITH SELECTIVELY APPLIED FUNCTIONAL AND TEST CLOCKS	SWOBODA, GARY L.
09943137	6912675	150	08/30/2001	USING SELECTIVE OMISSION TO COMPRESS ON-CHIP DATA PROCESSOR TRACE AND TIMING INFORMATION FOR EXPORT	SWOBODA, GARY L.
09943456	7206734	150	08/30/2001	EXPORTING ON-CHIP DATA PROCESSOR TRACE INFORMATION WITH VARIABLE PROPORTIONS OF CONTROL AND DATA	SWOBODA, GARY L.
09943595	Not Issued	95	08/30/2001	COLLECTING AND EXPORTING ON-CHIP DATA PROCESSOR TRACE AND TIMING INFORMATION WITH DIFFERING COLLECTION AND EXPORT FORMATS	SWOBODA, GARY L.
09943598	7043418	150	08/30/2001	SYNCHRONIZING ON-CHIP DATA PROCESSOR TRACE AND TIMING INFORMATION FOR EXPORT	SWOBODA, GARY L.
09943599	Not Issued	94	08/30/2001	CORRELATING ON-CHIP DATA PROCESSOR TRACE INFORMATION FOR EXPORT	SWOBODA, GARY L.
09943603	7076419	150	08/30/2001	USING SIGN EXTENSION TO COMPRESS ON-CHIP DATA	SWOBODA, GARY L.

				PROCESSOR TRACE AND TIMING INFORMATION FOR EXPORT	
09949265	7020600	150	09/07/2001	APPARATUS AND METHOD FOR IMPROVEMENT OF COMMUNICATION BETWEEN AN EMULATOR UNIT AND A HOST DEVICE	SWOBODA, GARY L.
10212550	Not Issued	161	08/05/2002	Apparatus and method for a reversible emulator/target cable connector	SWOBODA, GARY L.
10212621	6865504	150	08/05/2002	APPARATUS AND METHOD FOR A RECONFIGURABLE POD INTERFACE FOR USE WITH AN EMULATOR UNIT	SWOBODA, GARY L.

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